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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/574,030	03/27/2006	Robertus Theodorus Van Schaijk	NL03 1167 US1	8030

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EXAMINER	
HSIEH, HSIN YI	

ART UNIT	PAPER NUMBER
2811	

NOTIFICATION DATE	DELIVERY MODE
06/09/2011	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/574,030	VAN SCHAIJK ET AL.	
	Examiner	Art Unit	
	HSIN-YI HSIEH	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 December 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-8,10,11 and 13-19* is/are pending in the application.

4a) Of the above claim(s) *8, 10, 11, 13, 15, and 16* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-7,14 and 17-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. In view of the Appeal Brief filed on 12/22/2010, PROSECUTION IS HEREBY REOPENED. A new ground of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

/Lynne A. Gurley/

Supervisory Patent Examiner, Art Unit 2811.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. **Claim 3** is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Claim 3 recites the limitation "the dielectric material having an oxygen diffusion through the material that is an order of magnitude smaller than oxygen diffusion through oxide spacers includes one or more of silicon nitride, silicon carbide or metal oxide" which is in contrary to itself. The metal oxide is one of the materials of the oxide layer and it can not have an oxygen diffusion through the material that is an order of magnitude smaller than oxygen diffusion through oxide spacers.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. **Claims 1, 3, 5-7 and 17-19** are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (US 5,991,204 A) in view of Fan et al. (US 2004/0065917), and further in view of Quirk et al. ("Semiconductor Manufacturing Technology", 2001, Prentice Hall, pages 456 and 459-461).

8. Chang teaches, regarding to **claim 1**, a method of manufacturing on a substrate (semiconductor substrate 100; Fig. 1a, col. 3 line 58) a 2-transistor memory cell (Flash EEPROM cell; Abstract) comprising a storage transistor (the transistor formed under 101) having a memory gate stack (the gate stack under 101) and a selecting transistor (the transistor under 107), there being a tunnel dielectric layer (floating gate oxide layer 104; Fig. 1a, col. 4 lines 2-3) between the substrate (100) and the memory gate stack (the gate stack under 101), the method comprising: forming the memory gate stack (the gate stack under 101) by providing a first conductive layer (floating gate poly 103 in Fig. 6a before the etching) on the tunnel dielectric layer (104; see Fig. 1a) and a second conductive layer (second poly; col. 8 lines 55-58) with a deposited interlayer dielectric layer (layer 102 of ONO; Fig. 1a, col. 3 lines 64-65) between the first and second conductive layers (103 and 101; see Fig. 1a), the deposited interlayer dielectric layer (102) including oxide (oxide/nitride/oxide; col. 3 lines 64-65) and being susceptible to undesirable growth upon exposure to oxygen during subsequent oxidation steps (the interlayer dielectric layer 102 is between two polysilicon layers and is susceptible to undesirable growth if two polysilicon layers exposed to oxygen during subsequent oxidation steps), etching the second conductive layer (second poly) thus forming a control gate (101; Fig. 6a, col. 8 lines 55-58), forming spacers (control gate spacer 106; Fig. 6a, col. 8 lines 62-65) against the control gate (101) in the direction of a channel (active channel region 113; Fig. 1a, col. 3 line 62; the

direction of channel is the direction from the source to drain) to be formed under the tunnel dielectric layer (104; see Fig. 1a), and thereafter using the spacers (106) as a hard mask (col. 8 lines 62-65) to etch the first conductive layer (floating gate poly 103 in Fig. 6a before the etching) thus forming the floating gate (floating gate poly 103 in Fig. 6b after the etching), removing a portion of the tunnel dielectric (104) laterally adjacent to the floating gate (103) and exposing a portion of the substrate (100) where the tunnel dielectric (104) has been removed (see Fig. 6b, col. 9 lines 1-2); and forming an access gate dielectric oxide (erase gate oxide 112; Fig. 6c, col. 9 lines 3-4) on the exposed portion of the substrate (100; see Fig. 6c), using the spacers (106) to mitigate the diffusion of oxygen to the deposited interlayer dielectric layer (102; the spacer 106 covers the interlayer dielectric layer 102 that oxygen has to diffuse across the spacer before reaching the interlayer dielectric layer, which means the diffusion of oxygen to 102 is mitigated by the extra diffusing process across the spacer), and regarding to **claim 17**, a method of manufacturing a two-transistor memory cell (Flash EEPROM cell; Abstract) comprising a storage transistor (the transistor formed under 101) having a memory gate stack (the gate stack under 101) and a selecting transistor (the transistor under 107), the method comprising: forming a tunnel dielectric (floating gate oxide layer 104; Fig. 1a, col. 4 lines 2-3) on a substrate (semiconductor substrate 100; Fig. 1a, col. 3 line 58); forming a first conductive layer (floating gate poly 103 in Fig. 6a before the etching) on the tunnel dielectric (104; see Fig. 1a); depositing an interlayer dielectric layer (layer 102 of ONO; Fig. 1a, col. 3 lines 64-65) on the first conductive layer (103), the deposited interlayer dielectric layer (102) including oxide (oxide/nitride/oxide; col. 3 lines 64-65) and being susceptible to undesirable growth upon exposure to oxygen during subsequent oxidation steps (the interlayer dielectric layer 102 is

between two polysilicon layers and is susceptible to undesirable growth if two polysilicon layers exposed to oxygen during subsequent oxidation steps); forming a second conductive layer (second poly; col. 8 lines 55-58) on the interlayer dielectric layer (102; Fig. 1a); etching the second conductive layer (second poly) to form a control gate (101; Fig. 6a, col. 8 lines 55-58); forming a selecting transistor (the transistor under 107) on the substrate (100; Fig. 6c) laterally adjacent to the first conductive layer (103) and having an access gate (107) on an access gate dielectric (erase gate oxide 112; Fig. 6c, col. 9 lines 3-4); forming spacers (106) against sides of the control gate (101; Fig. 6a), one of the spacers (106) being formed between the control gate (101) and the access gate (107; see Fig. 6c); using the spacers (106) to mask underlying portions of the interlayer dielectric layer (102) and the first conductive layer (103; Fig. 6a), etching the first conductive layer (103) to form a floating gate (103; col. 8 lines 62-65); forming a floating gate sidewall dielectric (poly tunnel oxide 109; Fig. 6c, col. 9 lines 3-6) that is contiguous with the access gate dielectric (112; see Fig. 1a) and present between the floating gate (103) and the access gate (107; Fig. 1a), wherein the one of the spacers (106) being formed between the control gate (101) and the access gate (107) is thicker than the floating gate sidewall dielectric(109; see Fig. 1a); removing a portion of the tunnel dielectric (104) laterally adjacent to the floating gate (103) and exposing a portion of the substrate (100) where the tunnel dielectric (104) has been removed (see Fig. 6b, col. 9 lines 1-2); and forming an access gate dielectric oxide (erase gate oxide 112; Fig. 6c, col. 9 lines 3-4) on the exposed portion of the substrate (100; see Fig. 6c and col. 9 lines 3-4), using the spacers (106) to mitigate the diffusion of oxygen to the deposited interlayer dielectric layer (102; the spacer 106 covers the interlayer dielectric layer 102 that oxygen has to diffuse across the spacer before reaching the interlayer dielectric

layer, which means the diffusion of oxygen to 102 is mitigated by the extra diffusing process across the spacer).

Chang does not teach, regarding to **claim 1**, the spacers being formed from a dielectric material having an oxygen diffusion through the dielectric material that is, relative to oxide spacers, an order of magnitude smaller than oxygen diffusion through the oxide spacers, the etching of the first conductive layer being an anisotropic dry etch that is selective to the tunnel dielectric, thereby using the tunnel dielectric to protect portions of the substrate laterally adjacent to the floating gate; regarding to **claim 3**, the dielectric material having an oxygen diffusion through the material that is an order of magnitude smaller than oxygen diffusion through oxide spacers includes one or more of silicon nitride, silicon carbide or meal oxide, and regarding to **claim 17**, the spacers being formed from a dielectric material having an oxygen diffusion through the dielectric material that is, relative to oxide spacers, an order of magnitude smaller than oxygen diffusion through the oxide spacers, form a floating gate using an anisotropic dry etch that is selective to the tunnel dielectric, using the tunnel dielectric to mask portions of the substrate laterally adjacent to the floating gate.

In the same field of nonvolatile memory, Fan et al. teach, regarding to **claim 1**, the spacers (dielectric spacers 57; Fig. 6B, paragraph [0051]) being formed from a dielectric material (silicon nitride; paragraph [0051]) having an oxygen diffusion through the dielectric material that is, relative to oxide spacers, an order of magnitude smaller than oxygen diffusion through the oxide spacers (silicon nitride has the oxygen diffusion an order of magnitude small than that of the oxide), and regarding to **claim 3**, the dielectric material (silicon nitride; paragraph [0051]) having an oxygen diffusion through the material that is an order of magnitude smaller than

oxygen diffusion through oxide spacers includes one or more of silicon nitride, silicon carbide or meal oxide (silicon nitride), and regarding to **claim 17**, the spacers (dielectric spacers 57; Fig. 6B, paragraph [0051]) being formed from a dielectric material (silicon nitride; paragraph [0051]) having an oxygen diffusion through the dielectric material that is, relative to oxide spacers, an order of magnitude smaller than oxygen diffusion through the oxide spacers (silicon nitride has the oxygen diffusion an order of magnitude small than that of the oxide).

Fan et al. also teach that the silicon nitride is one of the materials for forming spacers on the sides of the control gate (paragraph [0051]).

In the same field of semiconductor manufacturing, Quirk et al. teach, regarding to **claim 1**, the etching of the first conductive layer (poly gate etch; Fig. 16.29, page 460, fourth paragraph) being an anisotropic dry etch (page 459, bottom paragraph and page 460, 4th paragraph) that is selective to the tunnel dielectric (i.e. gate oxide; page 460, 4th paragraph), thereby using the tunnel dielectric (gate oxide) to protect portions of the substrate laterally adjacent to the floating gate (avoiding any microtrenching of the gate oxide around the periphery of the polysilicon; page 460, the bottom paragraph), and regarding to **claim 17**, form a floating gate (poly gate, which can be a floating gate; Fig. 16.29, page 460, fourth paragraph) using an anisotropic dry etch (page 459, bottom paragraph and page 460, 4th paragraph) that is selective to the tunnel dielectric (i.e. gate oxide; page 460, 4th paragraph), using the tunnel dielectric (i.e. gate oxide) to mask portions of the substrate laterally adjacent to the floating gate (avoiding any microtrenching of the gate oxide around the periphery of the polysilicon; page 460, the bottom paragraph).

Quirk et al. also teach that dry etch can provides high selectivity and low device damage (page 456, the bottom two paragraphs).

It would have been obvious to one of ordinary skill in the art at the time of invention was made to combine the inventions of Chang, Fan et al., and Quirk et al. using the nitride spacers as taught by Fan et al. and the dry etch during the gate formation as taught by Quirk et al., because Chang is silent about the material of the spacers on the sides of the control gate while Fan et al. teach that the silicon nitride is one of the materials for forming spacers on the sides of the control gate (paragraph [0051]), and dry etch can provides high selectivity and low device damage as taught by Quirk et al. (page 456, the bottom two paragraphs).

9. Regarding **claim 5**, Chang also teaches a method according to claim 1, further including forming a floating gate dielectric (poly tunnel oxide 109; Fig. 6c, col. 9 lines 3-6) next to the formed floating gate (103) while forming the access gate dielectric (erased gate oxide 112; Fig. 6c, col. 9 lines 3-6).

10. Regarding **claim 6**, Chang also teaches a method according to claim 1, furthermore comprising removing part of the interlayer dielectric layer (102) after forming the control gate (this can be shown in Fig. 6a and Fig. 6b, where 102 is left only under the control gate 101) but before forming the spacers (this can be shown in Fig. 6a and Fig. 6b, where 102 is left only under the control gate 101 and is enclosed by the spacer 106).

11. Regarding **claim 7**, Chang also teaches a method according to claim 1 wherein, forming an access gate (107) includes forming the access gate while the spacer (106) at the access gate (107) side is still present (see Fig. 6c).

12. Regarding **claim 18**, Chang also teaches the method of claim 17, further comprising forming a cap layer (oxide cap 601; Fig. 6b, col. 8, lines 62-63) on the second conductive layer (101), wherein forming spacers (106) includes forming the one spacer (106), which is formed between the control gate (101) and the access gate (107; see Fig. 6c), between the cap layer (601) and the access gate (107) and in contact with the cap layer (601), the control gate (101), the access gate (107) and the floating gate (103; see Fig. 6c).

13. Regarding **claim 19**, Chang also teaches the method of claim 17, further comprising forming a cap layer (oxide cap 601; Fig. 6b, col. 8, lines 62-63) on the second conductive layer (101), wherein forming spacers includes forming the one spacer (the left 106), which is formed between the control gate (101) and the access gate (107; see Fig. 1a), between the cap layer (601) and the access gate (107) and in contact with the cap layer (601), the control gate (101), the access gate (107) and the floating gate (103; see Fig. 6c), further including forming another floating gate sidewall dielectric (109 at the right hand side of 103 in Fig. 6c) located on a sidewall (right sidewall) of the floating gate (103) opposite from the floating gate sidewall dielectric (109 at the left hand side of 103 in Fig. 6c), and further including forming offset spacers (106), one of the offset spacers (106 at the left hand side of 101 in Fig. 6c) being in contact with the access gate (107; see Fig. 6c), and another one of the offset spacers (106 at the right hand side of 101 in Fig. 6c) being in contact with the other floating gate sidewall dielectric (109 at the right hand side of 103 in Fig. 6c) and in contact with another one of the spacers (106 at the right hand side of 101 in Fig. 6c) that is located on a side (right side) of the control gate (101) opposite from the one spacer (106 at the left hand side of 101; see Fig. 6c).

14. **Claims 4 and 14** are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang, Fan et al., and Quirk et al. as applied to claim 1 above, and further in view of Hong et al. (US 5,614,746 A).

Chang teaches, regarding to **claim 4**, before forming the memory gate stack, applying the tunnel dielectric layer (104) on the substrate (100; this is shown in Fig. 6a), and after formation of the memory gate stack (see Fig. 6b), removing the tunnel dielectric layer (104) by a selective etching technique (stripping, col. 9 lines 1-2) at least at a location where the selecting transistor is to be formed (all the exposed area including the selecting transistor region; col. 9 lines 1-2), and regarding **claim 14**, removing a portion of the tunnel dielectric (104; see Fig. 6b, col. 9 lines 1-9) includes removing a portion of the tunnel dielectric laterally adjacent to the floating gate (103) and expose a portion of the substrate surface (100) (see Fig. 6b, col. 9 lines 1-9), and further including forming an access gate (erase gate 107; Fig. 6c, col. 4 line 7) of the selecting transistor (the transistor under 107) on the access gate dielectric (erase gate oxide 112; Fig. 6c, col. 9 lines 1-9).

Chang, Fan et al., and Quirk et al. do not teach, regarding to **claim 4**, the selective etching technique preferentially etching the tunnel dielectric layer compared to the substrate, and regarding to **claim 14**, wet etching the tunnel dielectric to remove a portion of the tunnel dielectric and expose a portion of the substrate surface where the tunnel dielectric has been wet etched, leaving the exposed surface of the substrate intact.

In the same field of nonvolatile memory, Hong et al. teach, regarding to **claim 4**, the selective etching technique (wet etching; Fig. 3E, col. 6 lines 58-61) preferentially etching the tunnel dielectric layer (tunnel oxide layer 22; Fig. 3E, col. 6 lines 58-61) compared to the

substrate (top surface of P-substrate 21; Fig. 3E, col. 6 lines 65-66), and regarding to **claim 14**, wet etching the tunnel dielectric (tunnel oxide layer 22; Fig. 3E, col. 6 lines 58-61) to remove a portion (exposed portion) of the tunnel dielectric (22) and expose a portion of the substrate surface (top surface of P-substrate 21; Fig. 3E, col. 6 lines 65-66) where the tunnel dielectric (22) has been wet etched (see Fig. 3E), leaving the exposed surface of the substrate intact (see Fig. 3E).

It would have been obvious to one of ordinary skill in the art at the time of invention was made to combine the inventions of Chang, Fan et al., Quirk et al. and Hong et al. to use the wet etch to remove the tunnel oxide because Chang, Fan et al., and Quirk et al. is silent of how to remove the tunnel oxide and Hong et al. provide a method of wet etch to remove the tunnel oxide.

Response to Arguments

15. Applicant's arguments with respect to claims 1, 3-7, 14, and 17-19 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HSIN-YI HSIEH whose telephone number is (571)270-3043. The examiner can normally be reached on Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne A. Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Lynne A. Gurley/
Supervisory Patent Examiner, Art Unit 2811

/H. H./
Examiner, Art Unit 2811
6/1/2011